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## Kahin Hai Mera Pyar Movie Download Mp4

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The present invention relates generally to the design of semiconductor devices, and more particularly to a non-volatile memory cell array design to be implemented in single-poly non-volatile memory, such as in EPROMs or EEPROMs. The size of the components in integrated circuits have reduced over the years and continues to reduce. Furthermore, the size of non-volatile memories, such as EPROMs or EEPROMs, has shrunk considerably in recent years. This is due to the fact that the trend in the semiconductor industry is to increase the density of memory cells on a chip, which in turn requires smaller cell areas. In order to reduce the size of the memory cell, the cell is made as small as possible. One type of cell structure that is commonly used for single poly non-volatile memories is shown in FIG. 1. This is a typical prior art architecture using a tunnel oxide layer 12, a floating gate layer 14, an interpoly dielectric layer 16 and a control gate layer 18. The structure is formed in a P-type substrate 10, with a P-well in substrate 10 and a deep N-well. As the cell is scaled down in size, the gate dimensions also scale down. In order to have a practical cell size, the cell size must be reduced at least to one micron, preferably below one micron. In addition to the cell size, the scalability of the cell is also an important issue in device design. When device dimensions are scaled down, problems arise in the cell scalability. For example, lithography, etching and ion implantation damage the tunnel oxide during scaling. The tunnel oxide breakdown voltage also decreases with decreasing cell dimensions. In order to compensate for the tunnel oxide breakdown voltage drop due to scaling, two independent poly capacitors must be used for a one-transistor cell. This is illustrated in FIG. 2. The poly A 12 is used for programming and reading, and the poly B 14 is used as a plate capacitor. The major problem is that the programming and reading voltages are doubled, which results in a higher power consumption and high programming and reading voltages. As a result, there is a limit to the scaling of the cell size.



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